AMENDMENTS TO THE SPECIFICATION:

Replace the paragraph at page 4, beginning at line 28, with the following amended paragraph:

The use of the dual port RAM 18 is preferred, as each interface 14 can access this memory without interfering with CPU 12 bus cycles. Locations within the dual port RAM 18 can be allocated to ~~individuals~~ individual ones of the IF 14 dynamically, with a programmable starting memory address and memory block size. Since all IF 14 data can be transferred between the interface and the dual port RAM 18, there is no need to transfer this data to the system memory 15, thereby improving the performance of the CPU 12. A block of dual port RAM memory 18 that is allocated to one of the IFs 14 can be operated in a block mode or in a FIFO mode wherein, by example, an associated one of the IF units 14 stores incoming data into the allocated block of dual port Ram 18, and the CPU 12 reads the stored data out in the first in, first out mode or, alternatively, the CPU 12 stores output data into the allocated block of dual port Ram 18, and the associated one of the IF units 14 reads the stored data out of the allocated block in the first in, first out mode.

Replace the paragraph at page 22, beginning at line 3 (Abstract of the Disclosure), with the following amended paragraph:

Disclosed is a programmable buffer circuit (16) for interfacing a CPU (12) to a plurality of channel interfaces (14). The buffer circuit includes a dual port memory (18) having a first port coupled to a CPU data bus and a second port coupled to a channel data bus that serves the plurality of channel interfaces. The buffer circuit further includes an arbitrator (24) for arbitrating access to the dual port memory by individual ones of the channel interfaces over the channel data bus; an address generator (26) for generating dual port memory addresses for reading and writing data using the CPU data bus and the channel data bus; and a control unit (20) and allocator (22) that are programmable by the CPU for specifying individual ones of buffer locations and sizes within the dual port memory for individual ones of the channel interfaces, and for enabling and disabling individual ones of the buffers. ~~The allocator has outputs coupled to the address~~

~~generator for controlling the generation of addresses thereby, depending on which channel interface is currently selected for access to the dual port memory. The control unit is programmable for operating individual ones of the channel buffers in a block access mode or in a first in/first out (FIFO) access mode of operation. In a preferred embodiment, at least the dual port memory, the CPU and the plurality of interface channels are contained within a common integrated circuit package, such as an ASIC. By example, one of the plurality of interface channels implements an audio CODEC, another one implements a serial data interface, and another one implements a packet data interface channel. Individual ones of the plurality of interface channels contain a receive interface and a transmit interface, and the allocator includes a corresponding plurality of registers for specifying at least a starting address and a size for each of of the receive interface and the transmit interface. The buffer circuit is also programmable for specifying a receive buffer of one channel interface to be a transmit buffer of another channel interface.~~